Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 4/8/16/32K Bytes of In-System Self-Programmable Flash program memory
  - 256/512/512/1K Bytes EEPROM
  - 512/1K/1K/2K Bytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    - Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package
    - Temperature Measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - 0 - 4 MHz@1.8 - 5.5V, 0 - 10 MHz@2.7 - 5.5.V, 0 - 20 MHz @ 4.5 - 5.5V
- Power Consumption at 1 MHz, 1.8V, 25°C
  - Active Mode: 0.2 mA
  - Power-down Mode: 0.1 µA
  - Power-save Mode: 0.75 µA (Including 32 kHz RTC)

8-bit AVR® Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash

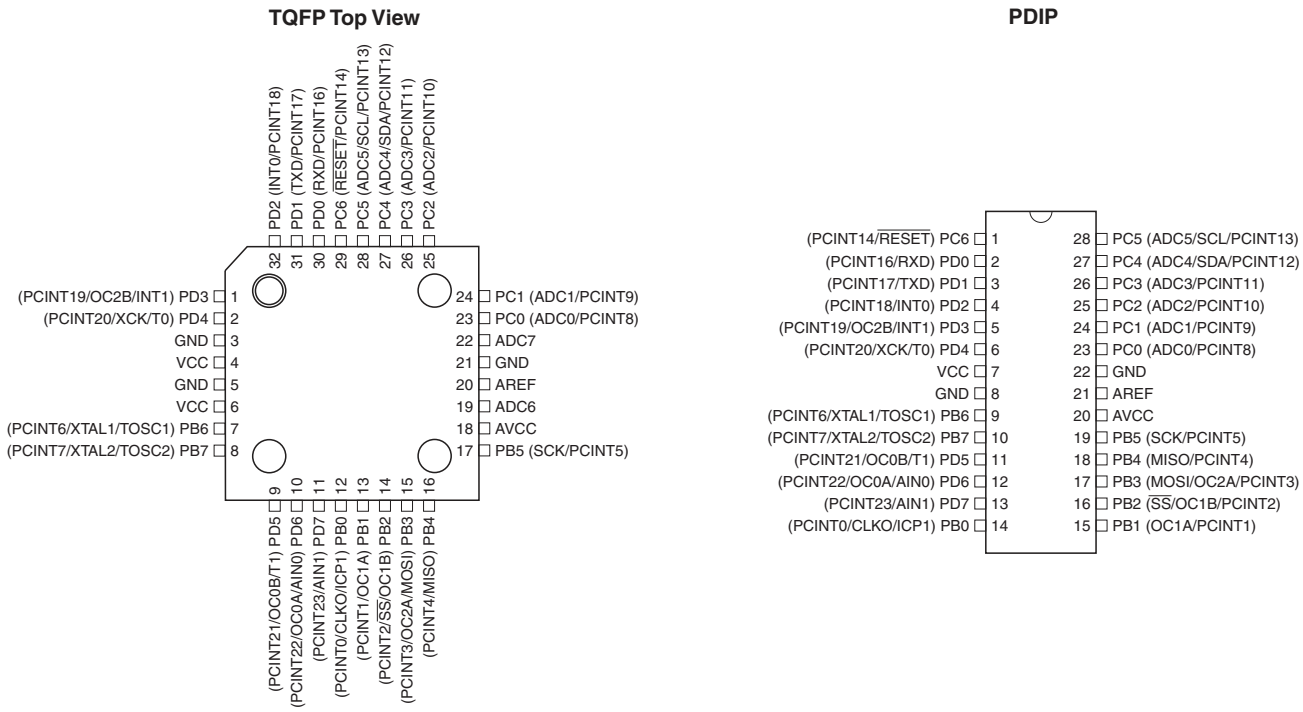
ATmega48A
ATmega48PA
ATmega88A
ATmega88PA
ATmega168A
ATmega168PA
ATmega328
ATmega328P

Summary

R . 8271BS, AVR, 04/10

1. Pin Configurations

Figure 1-1. P AT 48A/48PA/88A/88PA/168A/168PA/328/328P



1.1 Pin Descriptions

1.1.1 VCC

D

T [illegible] P [illegible] D [illegible] A [illegible] F [illegible] P [illegible] D [illegible] 89.

1.1.7 AV_{CC}

AV_{CC} [illegible] A/D C [illegible], PC3:0, [illegible] ADC7:6. I [illegible] [illegible] [illegible] V_{CC}, [illegible] ADC [illegible]. I [illegible] ADC [illegible], [illegible] [illegible] V_{CC} [illegible] - [illegible]. N [illegible] PC6...4 [illegible] [illegible], V_{CC}.

1.1.8 AREF

AREF [illegible] A/D C [illegible].

1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

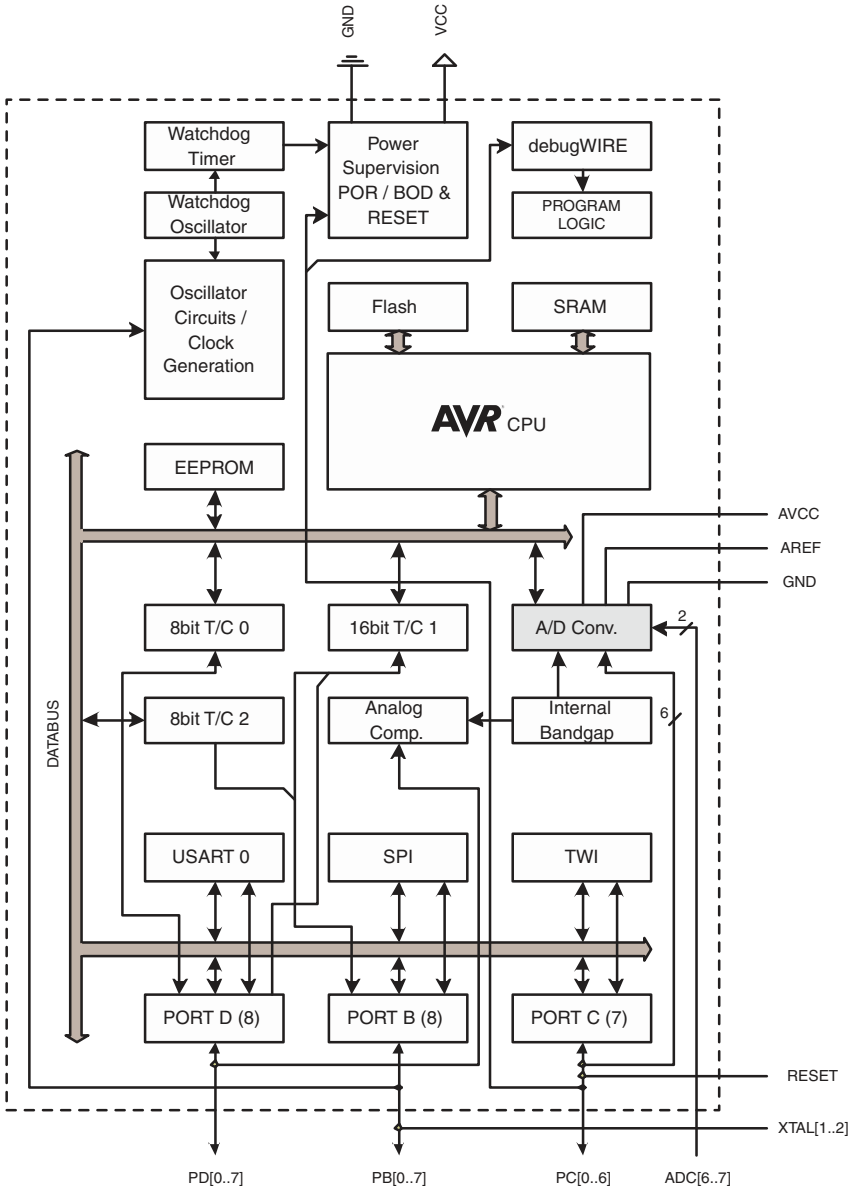
I [illegible] TQFP [illegible] QFN/MLF [illegible], ADC7:6 [illegible] [illegible] A/D [illegible] [illegible]. T [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] 10- ADC [illegible].

2. Overview

T AT 48A/48PA/88A/88PA/168A/168PA/328/328P - CMOS 8- -
AVR RISC . B
, AT 48A/48PA/88A/88PA/168A/168PA/328/328P -
1 MIPS MH
.

2.1 Block Diagram

Figure 2-1. B D



T AVR 32 32 . A
32 A L U (ALU),

T AT 48A/48PA/88A/88PA/168A/168PA/328/328P : 4K/8K I -S P F R -W -W , 256/512/512/1K EEPROM, 512/1K/1K/2K SRAM, 23 I/O , 32 T /C USART, - 2- S I , SPI , 6 10- ADC (8 TQFP QFN/MLF), - W T O , . T I CPU SRAM, T /C , USART, 2- S I , SPI , O , . T P - . I P - , 0 9 T 3 .07 II

Table 2-1. M ! S S !

Device	Flash	EEPROM	RAM	Interrupt Vector Size
AT 168PA	16K B	512 B	1K B	2 !$# ! / $# !
AT 328	32K B	1K B	2K B	2 !$# ! / $# !
AT 328P	32K B	1K B	2K B	2 !$# ! / $# !

AT 48A/48PA/88A/88PA/168A/168PA/328/328P ! ! R -W -W! S -P! -
! $# . T ! ! B L !S$# , SPM !$# $#
$# ! ! . I AT 48A/48PA ! R -W -W! ! !
! B L !S$# . T SPM !$# $# $# ! ! F .

3. Resources

A$# ! , $# ! !
:// . $# / !.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1D (0x3D)	EIMSK							INT1	INT0	73
0x1C (0x3C)	EIFR							INTF1	INTF0	73
0x1B (0x3B)	PCIFR						PCIF2	PCIF1	PCIF0	
0x1A (0x3A)	R									
0x19 (0x39)	R									
0x18 (0x38)	R									
0x17 (0x37)	TIFR2						OCF2B	OCF2A	TOV2	164
0x16 (0x36)	TIFR1			ICF1			OCF1B	OCF1A	TOV1	140
0x15 (0x35)	TIFR0						OCF0B	OCF0A	TOV0	
0x14 (0x34)	R									
0x13 (0x33)	R									
0x12 (0x32)	R									
0x11 (0x31)	R									
0x10 (0x30)	R									
0x0F (0x2F)	R									
0x0E (0x2E)	R									
0x0D (0x2D)	R									
0x0C (0x2C)	R									
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	94
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	94
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	94
0x08 (0x28)	PORTC		PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	93
0x07 (0x27)	DDRC		DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	93
0x06 (0x26)	PINC		PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	93
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	93
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	93
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	93
0x02 (0x22)	R									
0x01 (0x21)	R									
0x0 (0x20)	R									

N : 1. F

2. I/O R 0x00 - 0x1F SBI CBI . I SBIS SBIC .
3. S S F . N AVR , CBI SBI S F . T CBI SBI 0x00 0x1F .
4. W I/O IN OUT, I/O 0x00 - 0x3F . W I/O R LD ST , 0x20 . T AT 48A/48PA/88A/88PA/168A/168PA/328/328P 64 O IN OUT . F E I/O 0x60 - 0xFF SRAM, ST/STS/STD LD/LDS/LDD .
5. O AT 88A/88PA/168A/168PA/328/328P.
6. BODS BODSE P AT 48PA/88PA/168PA/328P

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	R , R!	A R !	R ← R + R!	Z,C,N,V,H	1
ADC	R , R!	A C !! R !	R ← R + R! + C	Z,C,N,V,H	1
ADIW	R ,K	A I W !	R :R ← R :R + K	Z,C,N,V,S	2
SUB	R , R!	S !# R !	R ← R - R!	Z,C,N,V,H	1
SUBI	R , K	S !# C ' R !	R ← R - K	Z,C,N,V,H	1
SBC	R , R!	S !# C !! R !	R ← R - R! - C	Z,C,N,V,H	1
SBCI	R , K	S !# C !! C ' R	R ← R - K - C	Z,C,N,V,H	1
SBIW	R ,K	S !# I ' W !	R :R ← R :R - K	Z,C,N,V,S	2
AND	R , R!	L # AND R !	R ← R • R!	Z,N,V	1
ANDI	R , K	L # AND R ! C	R ← R • K	Z,N,V	1
OR	R , R!	L # OR R !	R ← R R!	Z,N,V	1
ORI	R , K	L # OR R ! C	R ← R K	Z,N,V	1
EOR	R , R!	E# OR R !	R ← R ⊕ R!	Z,N,V	1
COM	R	O ' C	R ← 0 FF − R	Z,C,N,V	1
NEG	R	T ' C	R ← 0 00 − R	Z,C,N,V,H	1
SBR	R ,K	S B ( ) R !	R ← R K	Z,N,V	1
CBR	R ,K	C !B ( ) R !	R ← R • (0 FF - K)	Z,N,V	1
INC	R	I#	R ← R + 1	Z,N,V	1
DEC	R	D#	R ← R − 1	Z,N,V	1
TST	R	T ' !Z ! !M	R ← R • R	Z,N,V	1
CLR	R	C !R !	R ← R ⊕ R	Z,N,V	1
SER	R	S R !	R ← 0 FF	N	1
MUL	R , R!	M U	R1:R0 ← R R!	Z,C	2
MULS	R , R!	M S	R1:R0 ← R R!	Z,C	2
MULSU	R , R!	M S U	R1:R0 ← R R!	Z,C	2
FMUL	R , R!	F# M U	R1:R0 ← (R R!) << 1	Z,C	2
FMULS	R , R!	F# M S	R1:R0 ← (R R!) << 1	Z,C	2
FMULSU	R , R!	F# M S U	R1:R0 ← (R R!) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	'	R J	PC ← PC + ' + 1	N	2
IJMP		I !# J (Z)	PC ← Z	N	2
JMP[1]	'	D !# J	PC ← '	N	3
RCALL	'	R S ! C	PC ← PC + ' + 1	N	3
ICALL		I !# C (Z)	PC ← Z	N	3
CALL[1]	'	D !# S ! C	PC ← '	N	4
RET		S ! R !	PC ← STACK	N	4
RETI		I !! R !	PC ← STACK	I	4
CPSE	R ,R!	C ! , S 'E	' (R = R!) PC ← PC + 2 ! 3	N	1/2/3
CP	R ,R!	C !	R − R!	Z, N,V,C,H	1
CPC	R ,R!	C ! C !!	R − R! − C	Z, N,V,C,H	1
CPI	R ,K	C ! R ! I	R − K	Z, N,V,C,H	1
SBRC	R!,	S 'B R !C !	' (R!( )=0) PC ← PC + 2 ! 3	N	1/2/3
SBRS	R!,	S 'B R ! S	' (R!( )=1) PC ← PC + 2 ! 3	N	1/2/3
SBIC	P,	S 'B I/O R !C !	' (P( )=0) PC ← PC + 2 ! 3	N	1/2/3
SBIS	P,	S 'B I/O R ! S	' (P( )=1) PC ← PC + 2 ! 3	N	1/2/3
BRBS	,	B! # 'S F S	' (SREG( ) = 1) PC←PC+ + 1	N	1/2
BRBC	,	B! # 'S F C !	' (SREG( ) = 0) PC←PC+ + 1	N	1/2
BREQ	'	B! # 'E	' (Z = 1) PC ← PC + ' + 1	N	1/2
BRNE	'	B! # 'N E	' (Z = 0) PC ← PC + ' + 1	N	1/2
BRCS	'	B! # 'C !! S	' (C = 1) PC ← PC + ' + 1	N	1/2
BRCC	'	B! # 'C !! C !	' (C = 0) PC ← PC + ' + 1	N	1/2
BRSH	'	B! # 'S !H !	' (C = 0) PC ← PC + ' + 1	N	1/2
BRLO	'	B! # 'L !	' (C = 1) PC ← PC + ' + 1	N	1/2
BRMI	'	B! # 'M	' (N = 1) PC ← PC + ' + 1	N	1/2
BRPL	'	B! # 'P	' (N = 0) PC ← PC + ' + 1	N	1/2
BRGE	'	B! # 'G ! !E , S	' (N ⊕ V= 0) PC ← PC + ' + 1	N	1/2
BRLT	'	B! # 'L T Z !, S	' (N ⊕ V= 1) PC ← PC + ' + 1	N	1/2
BRHS	'	B! # 'H 'C !! F S	' (H = 1) PC ← PC + ' + 1	N	1/2
BRHC	'	B! # 'H 'C !! F C !	' (H = 0) PC ← PC + ' + 1	N	1/2
BRTS	'	B! # 'T F S	' (T = 1) PC ← PC + ' + 1	N	1/2
BRTC	'	B! # 'T F C !	' (T = 0) PC ← PC + ' + 1	N	1/2
BRVS	'	B! # 'O !' F S	' (V = 1) PC ← PC + ' + 1	N	1/2
BRVC	'	B! # 'O !' F C !	' (V = 0) PC ← PC + ' + 1	N	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
POP	R	P R ! 1 S ‘#	R ← STACK	N	2
MCU CONTROL INSTRUCTIONS					
NOP		N O !		N	1
SLEEP		S	(‘# ‘# ‘#. ‘ ! S ‘#)	N	1
WDR		W ‘# R	(‘# ‘# ‘#. ‘ ! WDR/ !)	N	1
BREAK		B!	F ! O ‘# D O	N	N/A

N : 1. T ! ‘# ! AT 168PA AT 328P.

6. Ordering Information

6.1 ATmega48A

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
20[3]	1.8 - 5.5	AT 48A-AU AT 48A-AUR[5] AT 48A-MMH[4] AT 48A-MMHR[4][5] AT 48A-MU AT 48A-MUR[5] AT 48A-PU	32A 32A 28M1 28M1 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N : 1. T P A
2. P E D R H S (R HS).A H G .
3. S S G 321.
4. NP A L F .
5. T & R .

Package Type	
32A	32- , T (1.0) P Q F P (TQFP)
28M1	28- , 4 4 1.0 , L P 0.45 Q F N -L /M L F P (QFN/MLF)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P (QFN/MLF)
28P3	28- , 0.300 W , P D I P (PDIP)

6.2 ATmega48PA

Speed (MHz)	Power Supply	Ordering Code [2]	Package [1]	Operational Range
20[3]	1.8 - 5.5	ATmega48PA-AU ATmega48PA-AUR[5] ATmega48PA-MMH[4] ATmega48PA-MMHR[4][5] ATmega48PA-MU ATmega48PA-MUR[5] ATmega48PA-PU	32A 32A 28M1 28M1 32M1-A 32M1-A 28P3	Industrial (-40°C to 85°C)

Note:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.
3. See ”Speed Grades” on page 321.
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28M1	28-pad, 4 x 4 x 1.0 body, Lead Pitch 0.45 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
28P3	28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)

6.3 ATmega88A

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
20[3]	1.8 - 5.5	AT 88A-AU	32A	I (-40°C 85°C)
		AT 88A-AUR[5]	32A	
		AT 88A-MMH[4]	28M1	
		AT 88A-MMHR[4][5]	28M1	
		AT 88A-MU	32M1-A	
		AT 88A-MUR[5]	32M1-A	
		AT 88A-PU	28P3	

N :
1. T P A .
2. P E D R H S (R HS).A H G .
3. S S G 321.
4. N P A L F .
5. T & R .

Package Type		
32A	32- , T (1.0) P Q F P (TQFP)	
28M1	28- , 4 4 1.0 , L P 0.45 Q F N -L /M L F P	(QFN/MLF)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P	(QFN/MLF)

6.4 ATmega88PA

Speed (MHz)	Power Supply (V)	Ordering Code[2]	Package[1]	Operational Range
20[3]	1.8 - 5.5	AT 88PA-AU AT 88PA-AUR[5] AT 88PA-MMH[4] AT 88PA-MMHR[4][5] AT 88PA-MU AT 88PA-MUR[5] AT 88PA-PU	32A 32A 28M1 28M1 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N : 1. T .P A .

2. P -E D R H S (R HS).A H G .
3. S S G 321.
4. NP A L F .
5. T & R .

Package Type	
32A	32- , T (1.0) P Q F P (TQFP)
28M1	28- , 4 4 1.0 , L P 0.45 Q F N -L /M L F P (QFN/MLF)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P (QFN/MLF)
28P3	28- , 0.300 W , P D I P (PDIP)

6.5 ATmega168A

Speed (MHz)[3]	Power Supply (V)	Ordering Code[2]	Package[1]	Operational Range
20	1.8 - 5.5	AT 168A-AU AT 168A-AUR[5] AT 168A-MMH[4] AT 168A-MMHR[4][5] AT 168A-MU AT 168A-MUR[5] AT 168A-PU	32A 32A 28M1 28M1 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N : 1. T P A A .

2. P E D R H S (R HS).A H G .
3. S S G 321
4. N P A L F .
5. T & R .

Package Type	
32A	32- , T (1.0) P Q F P (TQFP)
28M1	28- , 4 4 1.0 , L P 0.45 Q F N -L /M L F P (QFN/MLF)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P (QFN/MLF)
28P3	28- , 0.300 W , P D I P (PDIP)

6.6 ATmega168PA

Speed (MHz)[3]	Power Supply (V)	Ordering Code[2]	Package[1]	Operational Range
20	1.8 - 5.5	AT 168PA-AU AT 168PA-AUR[5] AT 168PA-MMH[4] AT 168PA-MMHR[4][5] AT 168PA-MU AT 168PA-MUR[5] AT 168PA-PU	32A 32A 28M1 28M1 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N : 1. T .P A .

2. P -F E D R H S (R HS).A H G .
3. S S G 321.
4. NP A L F .
5. T & R .

Package Type	
32A	32- , T (1.0) P Q F P (TQFP)
28M1	28- , 4 4 1.0 , L P 0.45 Q F N -L /M L F P (QFN/MLF)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P (QFN/MLF)
28P3	28- , 0.300 W , P D I P (PDIP)

6.7 ATmega328

Speed (MHz)	Power Supply (V)	Ordering Code[2]	Package[1]	Operational Range
20[3]	1.8 - 5.5	AT 328-AU AT 328-AUR[4] AT 328-MU AT 328-MUR[4] AT 328-PU	32A 32A 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N :
1. T
2. P E D R H S (R HS).A H G .
3. S F 28-1 321.
4. T & R

	Package Type
32A	32- , T (1.0) P Q F P (TQFP)
28P3	28- , 0.300 W , P D I P (PDIP)
32M1-A	32- , 5 5 1.0 , L P 0.50 Q F N -L /M L F P (QFN/MLF)

6.8 ATmega328P

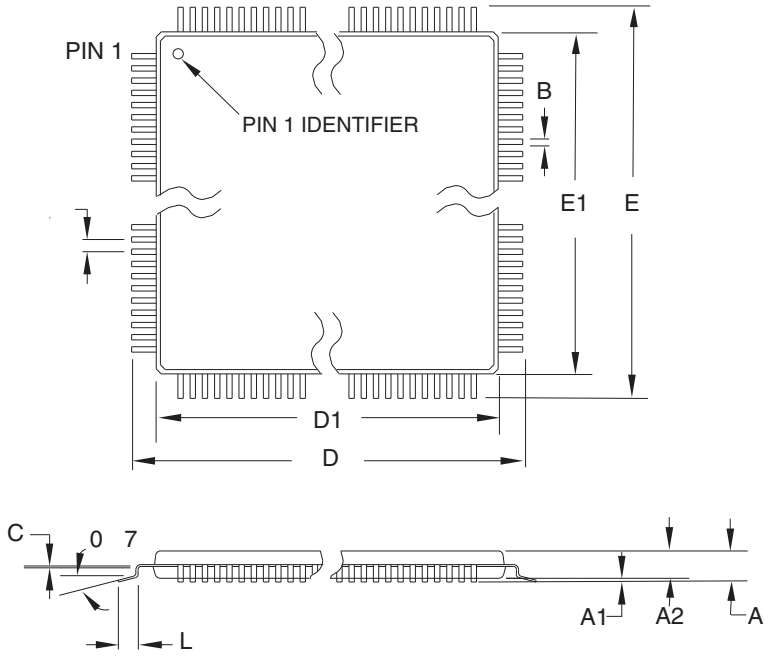
Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
20[3]	1.8 - 5.5	AT 328P-AU AT 328P-AUR[4] AT 328P-MU AT 328P-MUR[4] AT 328P-PU	32A 32A 32M1-A 32M1-A 28P3	I (-40°C 85°C)

N :
1. T P A .
2. P E D R H S (R HS).A H G .
3. S F 28-1 321.
4. T & R .

Package Type
32A

7. Packaging Information

7.1 32A



COMMON DIMENSIONS
(U M =)

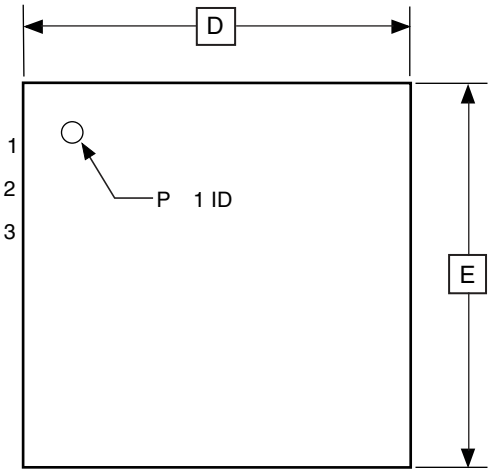
SYMBOL	MIN	NOM	MAX	NOTE
A			1.20	
A1	0.05		0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	N 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	N 2
B	0.30		0.45	
C	0.09		0.20	
L	0.45		0.75	
	0.80 TYP			

N : 1. T JEDEC MS-026, V ABA.
2. D D1 E1 . A
0.25 . D D1 E1
.
3. L 0.10

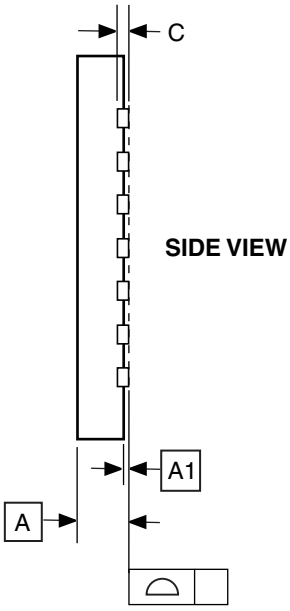
10/5/2001

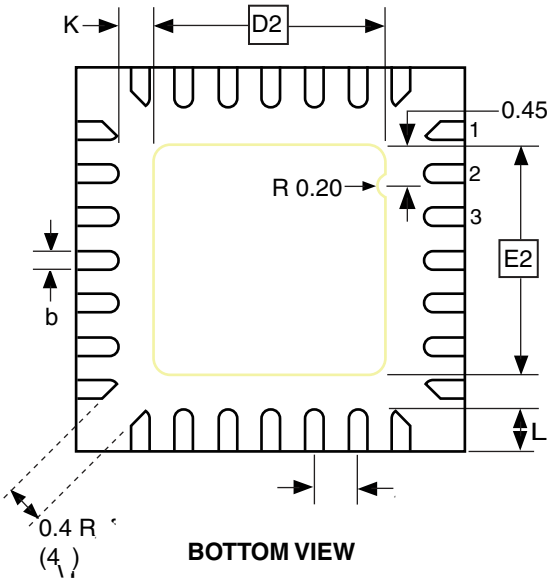
	TITLE	DRAWING NO.	REV.
2325 O P S J , CA 95131	**32A,** 32- , 7 7 B S , 1.0 B T , 0.8 L P , T P P Q F P (TQFP)	32A	B

7.2 28M1



TOP VIEW





BOTTOM VIEW

N : T #1 ID L F u .

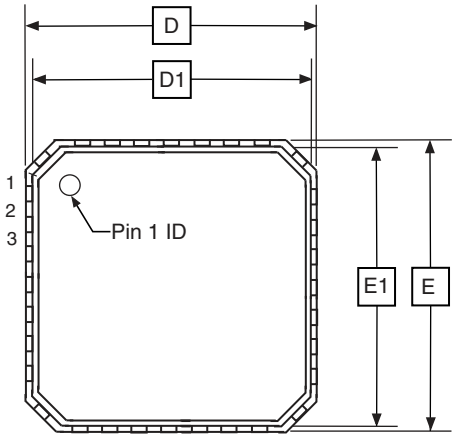
COMMON DIMENSIONS
(U M u =)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.17	0.22	0.27	
C		0.20 REF		
D	3.95	4.00	4.05	
D2	2.35	2.40	2.45	
E	3.95	4.00	4.05	
E2	2.35	2.40	2.45	
		0.45		
L	0.35	0.40	0.45	
	0.00		0.08	
K	0.20			

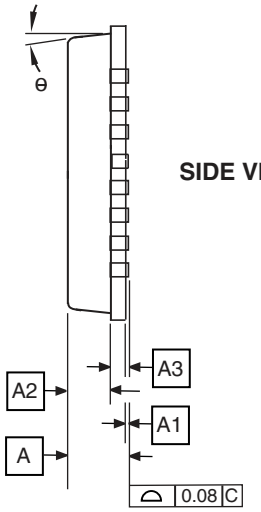
10/24/08

Package Drawing Contact:	TITLE	GPC	DRAWING NO.	REV.
w @	**28M1,** 28-pad, 4 x 4 x 1.0 mm Body, Lead Pitch 0.45 mm, 2.4 x 2.4 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	ZBV	28M1	B

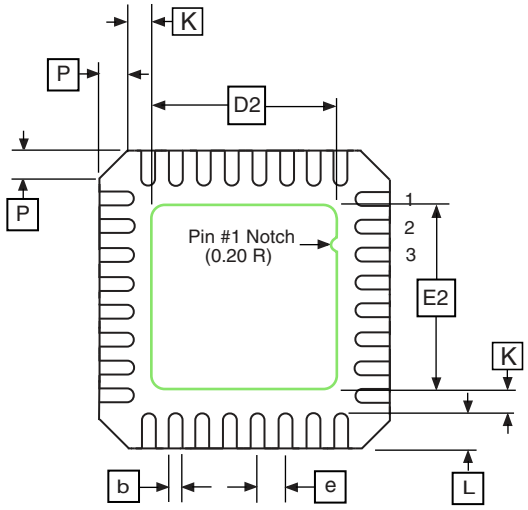
7.3 32M1-A



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

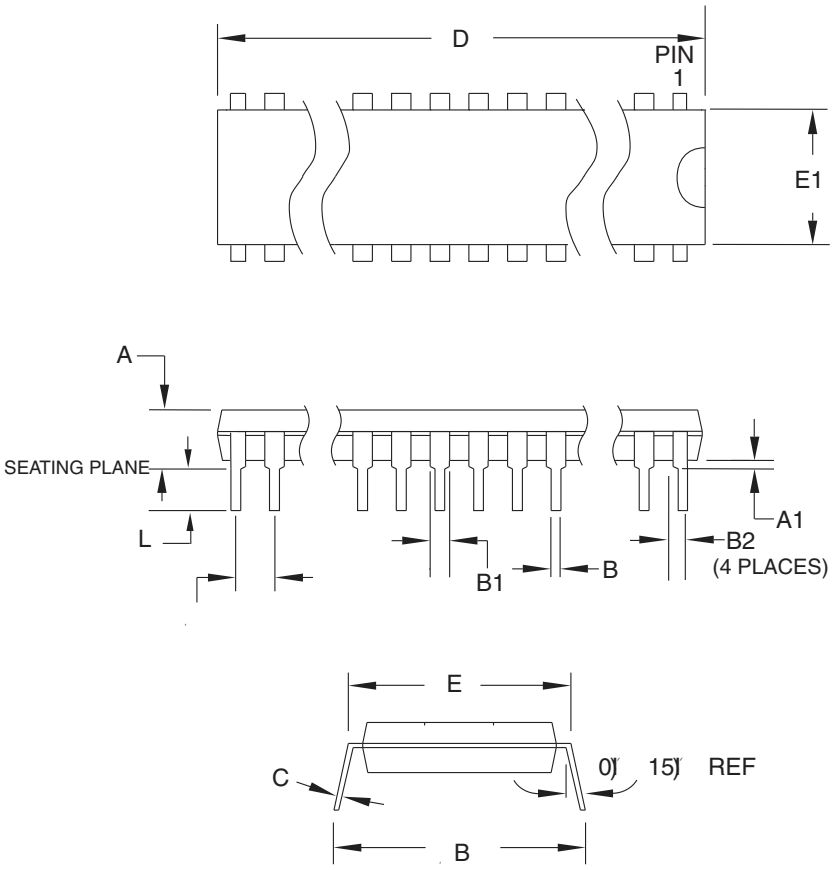
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, 3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	E

7.4 28P3



COMMON DIMENSIONS
(U M =)

SYMBOL	MIN	NOM	MAX	NOTE
A			4.5724	
A1	0.508			
D	34.544		34.798	N 1
E	7.620		8.255	
E1	7.112		7.493	N 1
B	0.381		0.533	
B1	1.143		1.397	
B2	0.762		1.143	
L	3.175		3.429	
C	0.203		0.356	
B			10.160	
	2.540 TYP			

N : 1. D D E1 # F P
M F P 0.25 (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 O # P S J , CA 95131	**28P3**, 28- (0.300"/7.62 W) P #D I P # (PDIP)	28P3	B

8. Errata

8.1 Errata ATmega48A

T ! ! #! ! ! AT 48A #.

8.1.1 Rev. D

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

I ACME (A C ! !M !E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ! ! " ACME #! .

Problem Fix/Workaround

C ! MUX3 ! ACME .

8.2 Errata ATmega48PA

T ! ! #! ! ! AT 48PA #.

8.2.1 Rev. D

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

I ACME (A C ! !M !E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ! ! " ACME #! .

Problem Fix/Workaround

C ! MUX3 ! ACME .

8.3 Errata ATmega88A

T ! ! #! ! ! AT 88A #.

8.3.1 Rev. F

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

I ACME (A C ! !M !E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ! ! " ACME #! .

Problem Fix/Workaround

C ! MUX3 ! ACME .

8.4 Errata ATmega88PA

T AT 88PA .

8.4.1 Rev. F

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

   I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

   Problem Fix/Workaround

   C MUX3 ACME .

8.5 Errata ATmega168A

T AT 168A .

8.5.1 Rev. E

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

   I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

   Problem Fix/Workaround

   C MUX3 ACME .

8.6 Errata ATmega168PA

T AT 168PA .

8.6.1 Rev E

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**

   I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

   Problem Fix/Workaround

   C MUX3 ACME .

8.7 Errata ATmega328

T AT 328 .

8.7.1 Rev D

Analog MUX can be turned off when setting ACME bit

1. Analog MUX can be turned off when setting ACME bit

I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

Problem Fix/Workaround

C MUX3 ACME .

8.7.2 Rev C

N .

8.7.3 Rev B

Analog MUX can be turned off when setting ACME bit

Unstable 32 kHz Oscillator

1. Unstable 32 kHz Oscillator

I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

Problem Fix/Workaround

C MUX3 ACME .

2. Unstable 32 kHz Oscillator

T 32 H . T 32 H -

Problem Fix/ Workaround

N .

8.7.4 Rev A

Analog MUX can be turned off when setting ACME bit

Unstable 32 kHz Oscillator

1. Unstable 32 kHz Oscillator

I ACME (A C M E) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1), MUX ACME .

Problem Fix/Workaround

C MUX3 ACME .

2. Unstable 32 kHz Oscillator

T 32 H . T 32 H -

Problem Fix/ Workaround

N .

8.8 Errata ATmega328P

T [illegible] AT 328P [illegible].

8.8.1 Rev D

Analog MUX can be turned off when setting ACME bit

1. **Analog MUX can be turned off when setting ACME bit**
   I[illegible] ACME (A C [illegible] M [illegible] E [illegible]) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1[illegible]), MUX [illegible] ACME [illegible].

   Problem Fix/Workaround
   C [illegible] MUX3 [illegible] ACME .

8.8.2 Rev C

N [illegible].

8.8.3 Rev B

Analog MUX can be turned off when setting ACME bit
Unstable 32 kHz Oscillator

1. **Unstable 32 kHz Oscillator**
   I[illegible] ACME (A C [illegible] M [illegible] E [illegible]) ADCSRB MUX3 ADMUX 1 (ADMUX[3:0]=1[illegible]), MUX [illegible] ACME [illegible].

   Problem Fix/Workaround
   C [illegible] MUX3 [illegible] ACME .

2. **Unstable 32 kHz Oscillator**
   T 32 H [illegible]. T 32 H [illegible] -[illegible].

   Problem Fix/ Workaround
   N .

8.8.4 Rev A

Unstable 32 kHz Oscillator

1. **Unstable 32 kHz Oscillator**
   T 32 H [illegible]. T 32 H [illegible] -[illegible].

   Problem Fix/ Workaround
   N .

9. Datasheet Revision History

P [illegible] T [illegible]

9.1 Rev. 8271B-04/10

1. U [illegible] T [illegible] 8-8 [illegible] 2/ 2
2. C [illegible] SBIS [illegible] .
3. C [illegible] BOD BODSE R/W S [illegible] 9.11.2 45, S [illegible] 11.5 69 S [illegible] 13.4 93
4. F [illegible], F [illegible] 29-34 349, F [illegible] 29-81 374, F [illegible] 29-128 399, F [illegible] 29-175 424, F [illegible] 29-222 449, F [illegible] 29-269 474, F [illegible] 29-316 499 F [illegible] 29-363 523.
5. U [illegible] P [illegible] I [illegible] 546 [illegible] 28M1 [illegible]

9.2 Rev. 8271A-12/09

1. N [illegible] 8271 [illegible] AT 48PA, AT 88PA, AT 168PA AT 48A, AT 88A AT 168A. A [illegible] AT 328 AT 328P
2. C :
   - N [illegible] : AT 48A/AT 88A/AT 168A AT 328
   - U F [illegible] D [illegible]
   - U T 2-1 6
   - A [illegible] BOD D 40.
   - A BOD BODSE MCUCR MCU C [illegible] R [illegible] 93 R [illegible] D [illegible] 294
   - A [illegible] B L [illegible] S [illegible] R -W -W[illegible] S -P[illegible] 279
   - A [illegible] P[illegible] A D M [illegible] L [illegible] B 296
   - A [illegible] DC [illegible]
   - A [illegible]
   - R [illegible] A [illegible] M [illegible] U 223.